



Product Data Sheet

FCF500

Release version 1.0

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RF Front end IC

Contact information

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Revision History

Version	Date	Description
Ver. 0.1	2016.12.20	Initial release.
Ver. 0.2	2017.01.09	POD & Application schematic 및 Pin configuration 수정
Ver. 0.3	2017.03.31	Application schematic 및 General Performance 수정
Ver. 1.0	2017.06.15	Application schematic 및 General Performance 수정

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1. Introduction

FCF500 is primarily designed for a TDD-mode RF front-end operated in the 800/900MHz frequency bands. FCF500 integrates a linear PA, LNA, Transmit and Receive switching circuitry and associated matching networks all in a CMOS single-chip device.

FCF500 provides superior output power , high power efficiency at Tx part and low noise figure , small current consumption at Rx part . FCF500 can be used for multiple applications in the sub-GHz bands from 850 to 950MHz.

FCF500 is manufactured with a CMOS process, and is packaged in a lead-free small package, named 3.0mm x 3.0mm QFN and this chipset requires minimal external components including the power supply bypass capacitors.

2. Feature

Item	Content
Frequency Range	UHF 850~950MHz
RX NF	2.0dB
RX current	10mA
TX Psat	+24.5dBm
TX current @ 23dBm	145mA
Size	16-pins QFN : 3.0mm × 3.0mm × 0.55mm

3. Block Diagram

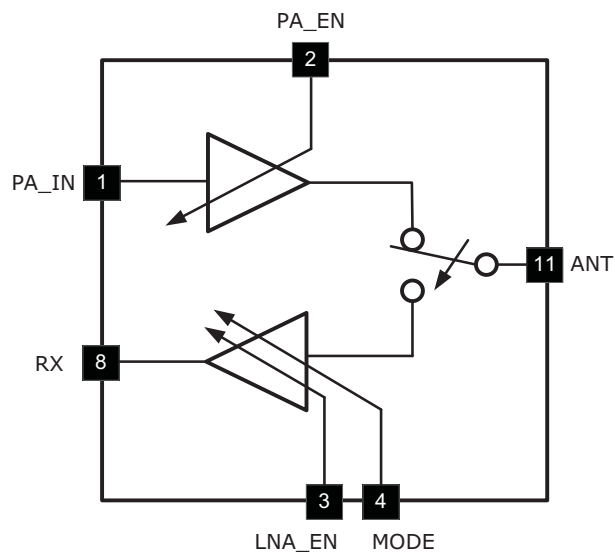


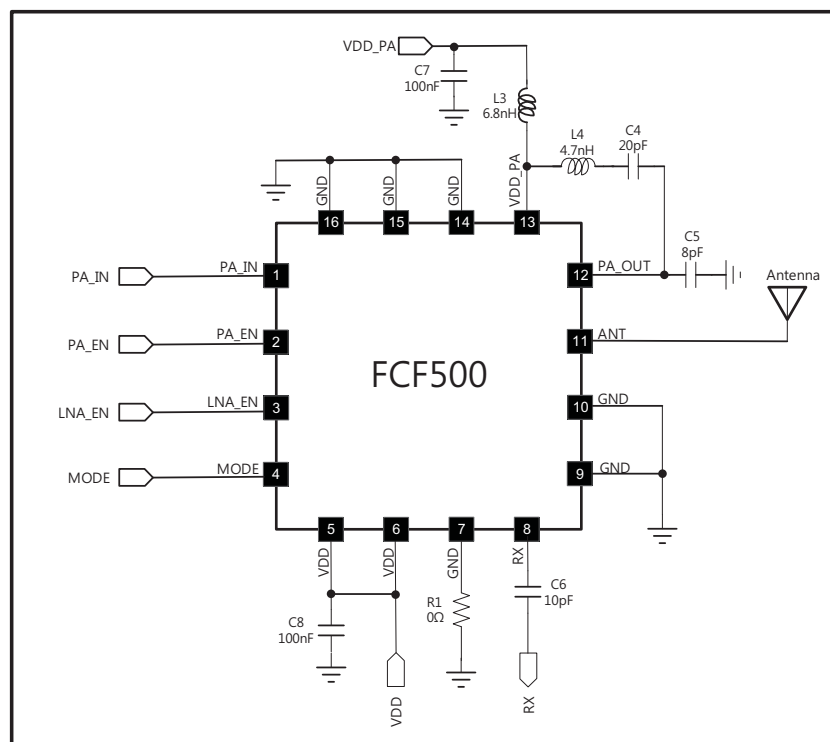
Figure 1. FCF500 Block Diagram

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4. Pin Configuration

Pin No.	Pin Name	Type	Description
1	PA_IN	Input	RF TX Signal from the Transceiver to the PA
2	PA_EN	Input	Input to Enable Transmit Mode
3	LNA_EN	Input	Input to Enable Receive Mode
4	MODE	Input	Input to Control High Gain /Low Gain for RX
5	VDD	Input	Voltage supply connection for logic block
6	VDD	Input	Voltage supply connection for the LNA
7	GND	GND	Ground
8	RX	Output	RF RX Signal from the LNA to the Receiver
9	GND	GND	Ground
10	GND	GND	Ground
11	ANT	Common	Common RF port Connected to the Antenna
12	PA_OUT	output	PA output
13	VDD_PA	Input	Voltage supply connection for the PA
14	GND	GND	Ground
15	GND	GND	Ground
16	GND	GND	Ground

5. Application Schematic



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